CMS8S006 Datasheet

Enhanced flash memory 1T 8051 microcontrollers

Rev. 0.1.4

Please note the following CMS IP policy

1. Product Features

1.1 Features

- **Compatible with MCS-51 1T instruction set**
  - Maximum system clock frequency supports up to 48 MHz.
  - Fastest machine cycle supports $1T_{SYS}$ @ F_{SYS}=16MHz
  - Fastest machine cycle supports $2T_{SYS}$ @ F_{SYS}=24MHz
  - Fastest machine cycle supports $3T_{SYS}$ @ F_{SYS}= 48MH
- **Memory**
  - Maximum program FLASH: 32K×8Bit
  - Maximum Data FLASH: 1K×8Bit
  - Universal RAM: 256×8Bit
  - Maximum universal XRAM: 2K×8Bit
  - Program/Data FLASH supports partition protection
- **Four oscillation modes**
  - HIS internal high-speed oscillation: 48MHz
  - HSE external high-speed oscillation: 8MHz/16MHz
  - LSE external low-speed oscillation: 32.768KHz
  - LSI internal low-speed oscillation: 125KHz
- **Low voltage reset function (LVR)**
  - 1.8V/2.0V/2.5V
- **Low voltage detection function (LVD)**
  - 2.0V/2.2V/2.4V/2.7V/3.0V/3.7V/4.0V/4.3V
- **GPIO**
  - Up to 30 GPIOs, supporting arbitrary allocation of digital functions
  - Support pull-up/pull-down resistor functionality
  - Support edge (rising/falling/both edges) interrupt and wake-up functions
- **Interrupt sources**
  - Support all external port interrupts, 8 timer interrupts.
  - Other peripheral interrupts
- **Timers**
  - WDT/WWDT timers (watchdog/windowed watchdog timer)
  - 5 general-purpose timers: Timer0/1, Timer2, Timer3/4
  - LSE Timer (supports sleep wake-up function)
  - WUT (wake-up timer)
- **Operating voltage range**
  - 2.1V~5.5V
- **Operating temperature range**
  - -40℃~85℃
- **Buzzer driver**
  - 50% duty cycle: frequency can be freely set
- **Enhanced PWM**
  - 6-channel enhanced PWM
  - 6 independent period counters
  - Mode support: independent, complementary, synchronous, and group modes
  - Support edge-aligned and center-aligned modes
  - Dead time function: supports dead time delay in complementary mode
  - Support masking function and fault protection function
- **High-precision 12-bit ADC**
  - All GPIOs (30 I/Os) support ADC channels
  - Sample and hold circuit: sampling rate up to 320 Ksps
  - Selectable reference voltage: options are 2.0V, 2.4V, 3.0V, and VDD.
  - Can detect an internal 1.2V reference voltage
  - Support hardware-triggered conversion startup
- **2-channel analog comparator (ACMP0/1)**
  - Positive terminal selection: 5 selectable channels; negative terminal can select internal 1.2V/VDD divider
  - Comparator supports single-edge and double-edge hysteresis
  - Hysteresis voltage: 10/20/60mV
  - Comparison output can trigger EPWM brake
  - Negative terminal input: internal 1.2V/VDD divider can connect to internal ADC channel
- **2-channel operational amplifiers (OP0/1)**
  - GPIO multiplexing: operational amplifier ports are multiplexed with GPIO ports.
  - Positive terminal input: supports internal 1.2V input
  - Support operational amplifier and comparator modes.
  - Operational amplifier output can connect to internal ADC channels

- BRT (UART baud rate clock generator)

◆ **Multiplication/Division Unit (MDU)**
- Support 32bit/16bit, 16bit/16bit, 16bit×16bit

◆ **Communication modules**
- 1xSPI (communication speed up to 6Mb/s)
- 1xI2C (communication speed up to 400Kb/s)
- 2xUART (baud rate up to 1Mb/s)

◆ **Support for dual-line/single-line serial programming and debugging**

- Operational amplifier output can connect to internal analog comparator inputs

◆ **Programmable Gain Amplifier (PGA)**
- Selectable gain amplification (1/2/4/8/16/32/64/128x)
- Supports single-ended and pseudo-differential inputs
- PGA output can connect to internal analog comparator inputs

◆ **96-bit Unique ID (UID)**
- Each chip has a distinct ID number

◆ **Low power modes**
- Idle mode 1/2 (IDLE1/2)
- Sleep mode (STOP)

1.2 Product comparison

Peripheral interface \ Product model		CMS8S006 DC20SA	CMS8S006 DC24SS	CMS8S006 DC24NA	CMS8S006 DC32FP	CMS8S006 DC32NA
Maximum clock frequency		48 MHz				
Memory module	APROM	32KB				
	BOOT	1/2/4KB				
	Data FLASH	1 KB				
	RAM	256 B				
	XRAM	2 KB				
Timer	WDT	1				
	WWDT	1				
	Timer0/1	2 (16bit)				
	Timer2	1 (16bit)				
	Timer3/4	2 (16bit)				
	LSE Timer	1 (16bit)				
	WUT	1 (12bit)				
	BRT	1 (16bit)				
Enhanced digital peripherals	BUZZER	1				
	MDU	32bit/16bit, 16bit/16bit, 16bit*16bit				
	PWM	6(16bit)				
Communication module	SPI	1				
	I2C	1				
	UART	2				
Analog module	12bit-ADC (Number of external channels)	18	22	22	30	30
	ACMP	Up to 2[1)]				
	OP	Up to 2[1)]				
	PGA	Up to 1[1)]				
GPIOs		30[1)]				
LVR		1.8V/2.0V/2.5V				
LVD		2.0V/2.2V/2.4V/2.7V/3.0V/3.7V/4.0V/4.3V				
Operating voltage		2.1~5.5 V				
Operating temperature		-40~85℃				
Package		TSSOP20	SSOP24	QFN24	LQFP32	QFN32

Note: 1) Subject to the actual chip.

2. System Overview

2.1 System introduction

The CMS8S006 is an 8051-core microcontroller compatible with the MCS-51 instruction system, featuring a general-purpose 8-bit architecture and a maximum operating frequency of up to 48 MHz. The MCU has the following characteristics:

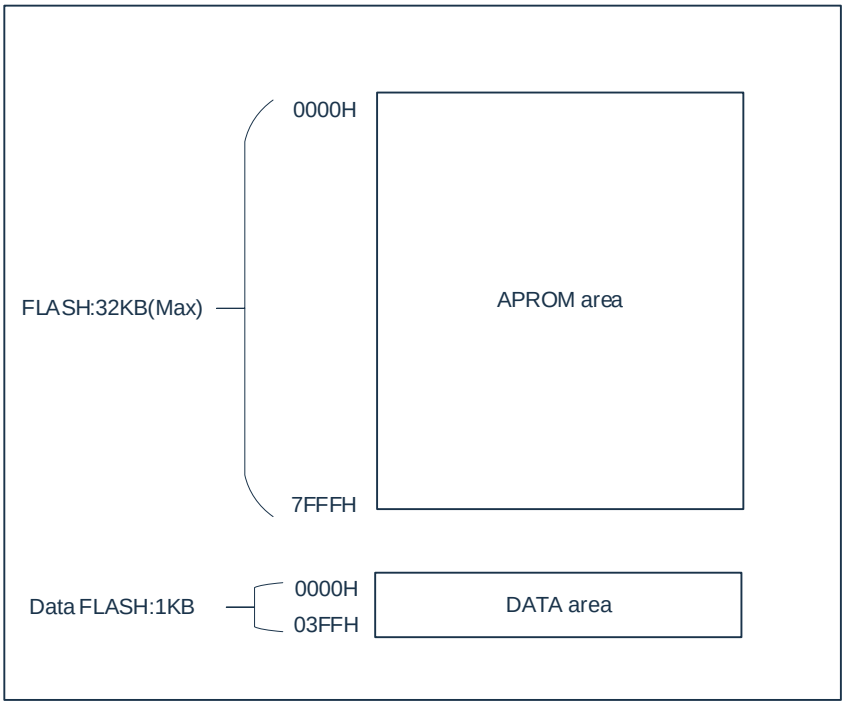
- Memory: Supports a maximum of 32KB program memory, 256B RAM, 2KB XRAM, and 1KB data memory.
- Oscillation modes: Offers four different oscillation modes.
- Power modes: Supports four operating modes: Normal, Idle Mode 1 (IDLE1), Idle Mode 2 (IDLE2), and Sleep Mode, effectively reducing power consumption.
- Protection features: Includes low-voltage reset (LVR), low-voltage detection (LVD), watchdog overflow reset, and window watchdog reset, enhancing system reliability.
- Interrupt sources: Provides multiple interrupt sources, including external interrupts, timer interrupts, and other peripheral interrupts, enabling timely responses to external events and improving MCU utilization.
- Digital functions can be assigned to any I/O port.
- Equipped with multiple timers capable of performing system resets, timing, counting, input capture, output comparison, timed wake-ups, and baud rate generation.
- Features a dedicated hardware unit for multiplication and division.
- Offers 6 channels of 16-bit PWM with support for independent, complementary, and synchronous output modes, along with hardware brake functionality, dead time control, and masked output options.
- 1 I2C module, 1 SPI module, and 2 UART modules for data transmission between the system and other devices.
- Contains a high-precision 12-bit ADC with selectable internal reference voltage, 2 operational amplifiers, 2 comparators, and 1 programmable gain amplifier, allowing each I/O to serve as an ADC input channel for enhanced analog functionality.

2.2 Memory mapping

2.2.1 FLASH memory

The series features a maximum of 32KB of FLASH storage space, with the APROM area and BOOT area sharing the entire FLASH space.

Below is a structural diagram illustrating the allocation of FLASH space:

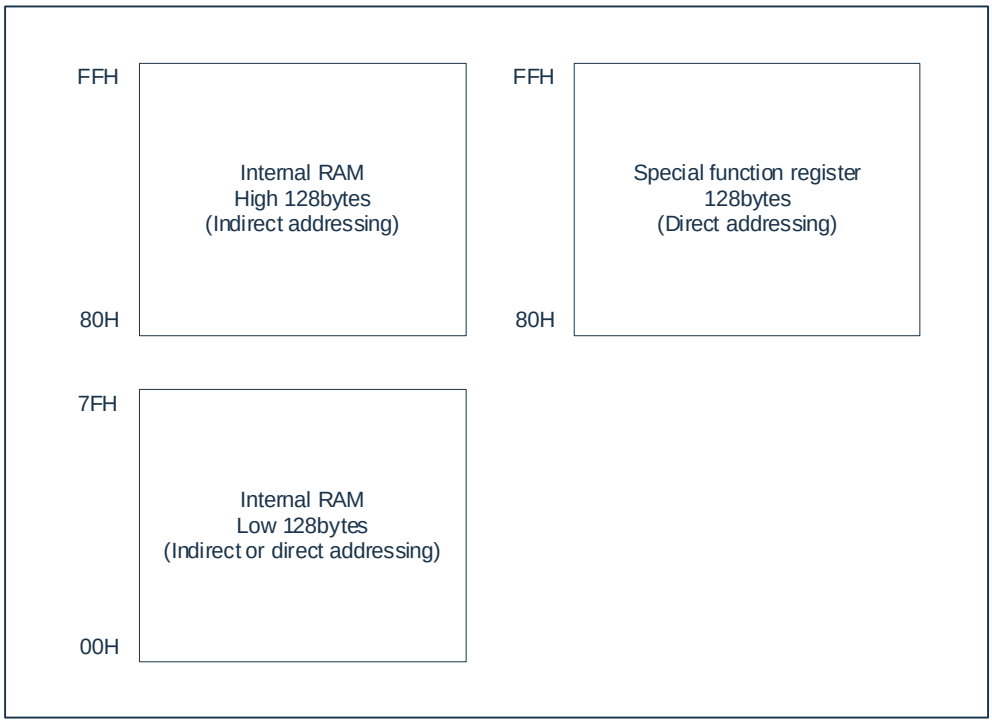


The BOOT size of the CMS8S006 can be configured, and the configuration method is as follows:

Program storage area				
Address space allocation method	APROM area		BOOT area	
Method 0	32K	0000H-7FFFH	--	--
Method 1	31K	0000H-7BFFH	1K	7C00H-7FFFH
Method 2	30K	0000H-77FFH	2K	7800H-7FFFH
Method 3	28K	0000H-6FFFH	4K	7000H-7FFFH

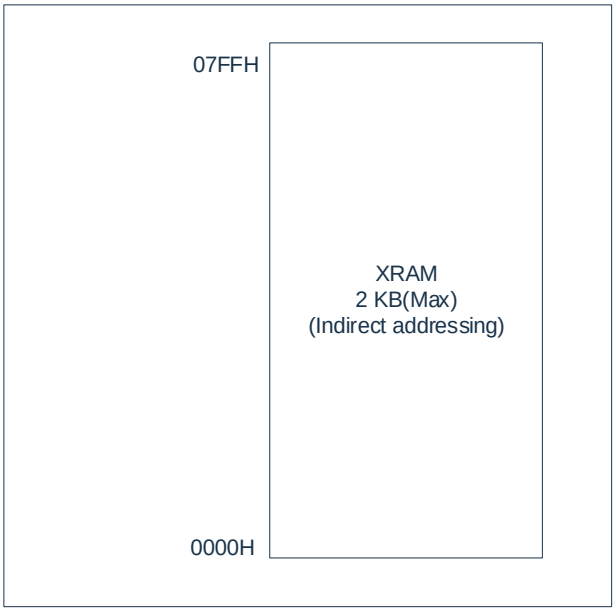
2.2.2 Internal data memory (RAM)

The internal data memory is divided into three parts: Low 128 Bytes, High 128 Bytes, and Special Function Registers (SFR). The RAM space allocation structure is illustrated in the diagram below:



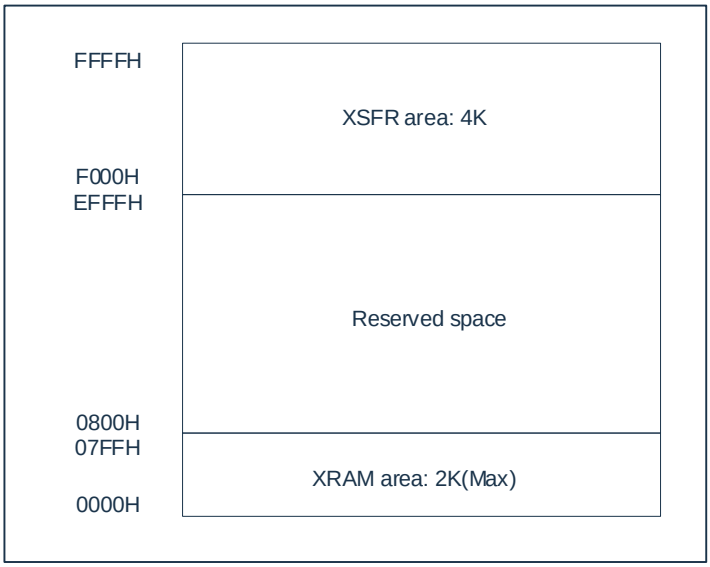
2.2.3 External data memory (XRAM)

The chip has a maximum of 2KB XRAM area, which is independent of the RAM/FLASH. The XRAM space allocation structure is illustrated in the diagram below:



2.2.4 Special function register (XSFR)

XSFR is a special register that shares the addressing space with XRAM. It primarily includes port control registers and other functional control registers. Its addressing range is as follows:

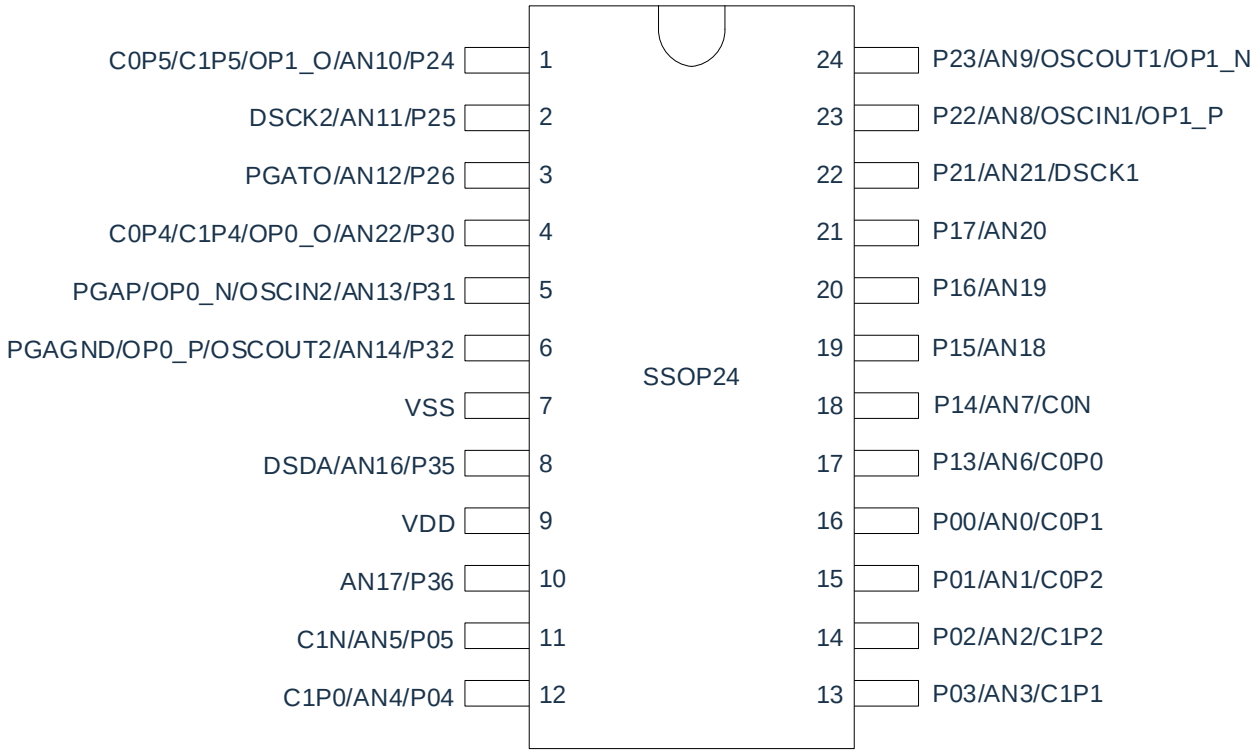


3. Pin Definition

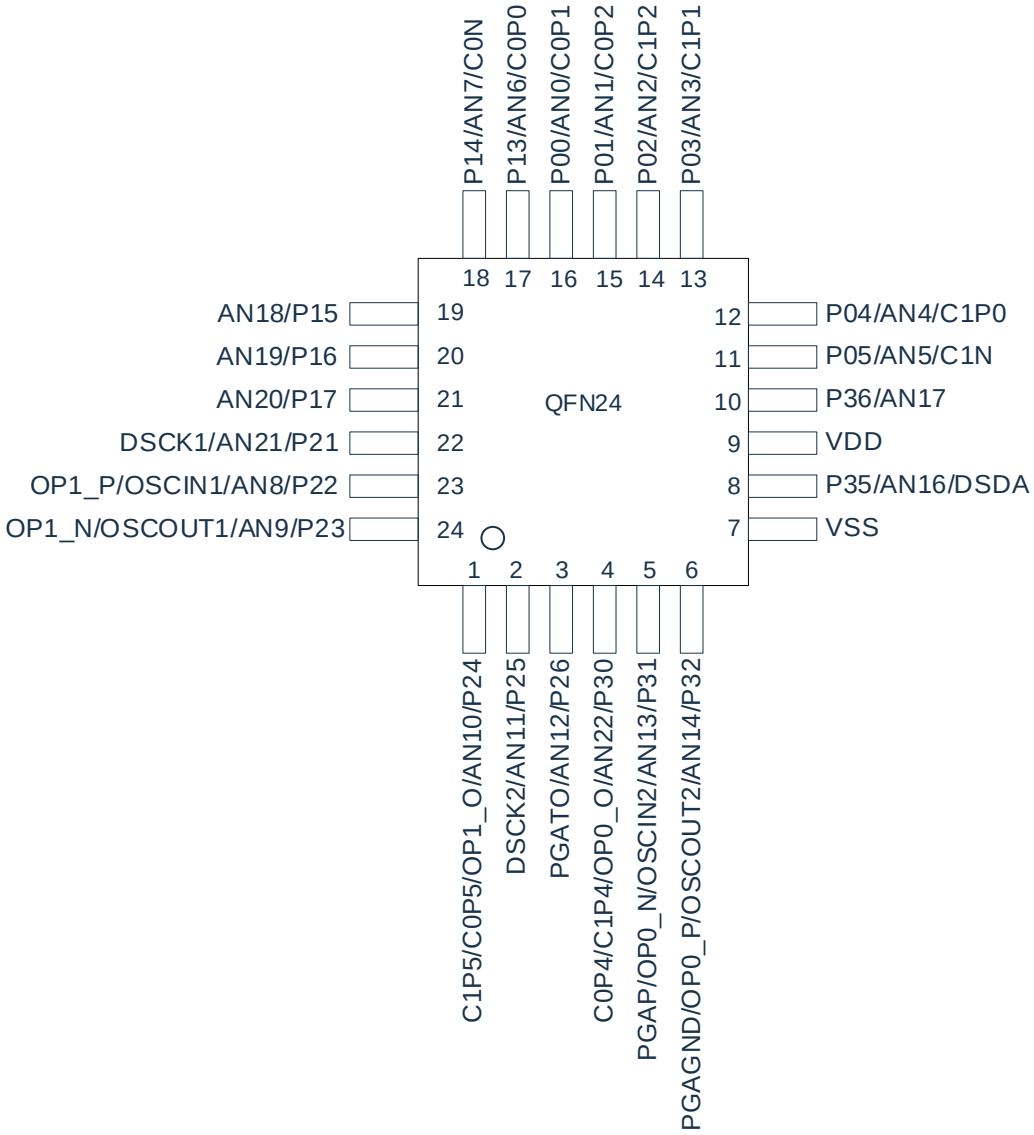
3.1 Top view

3.1.1 CMS8S006DC20SA

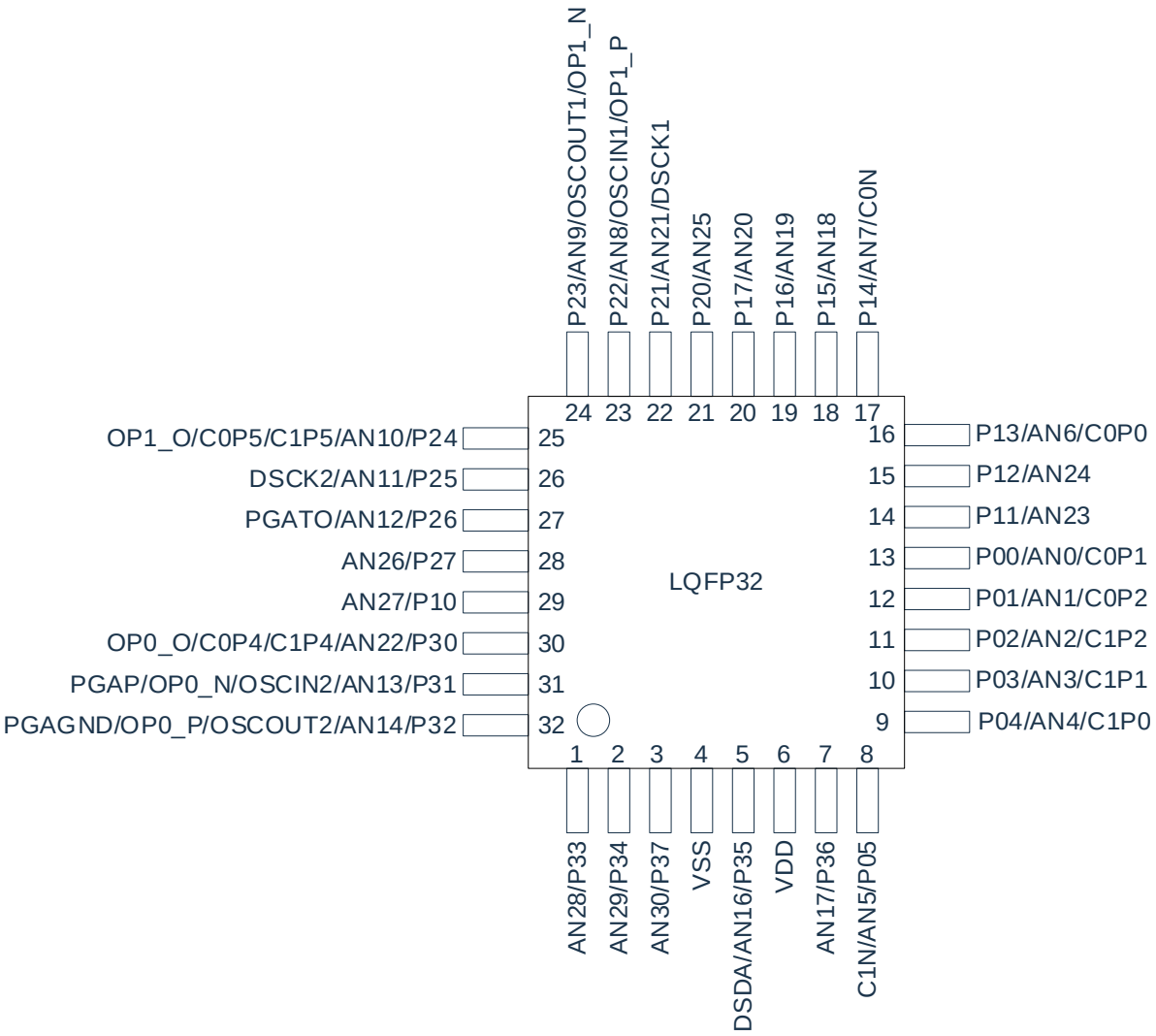
3.1.2 CMS8S006DC24SS



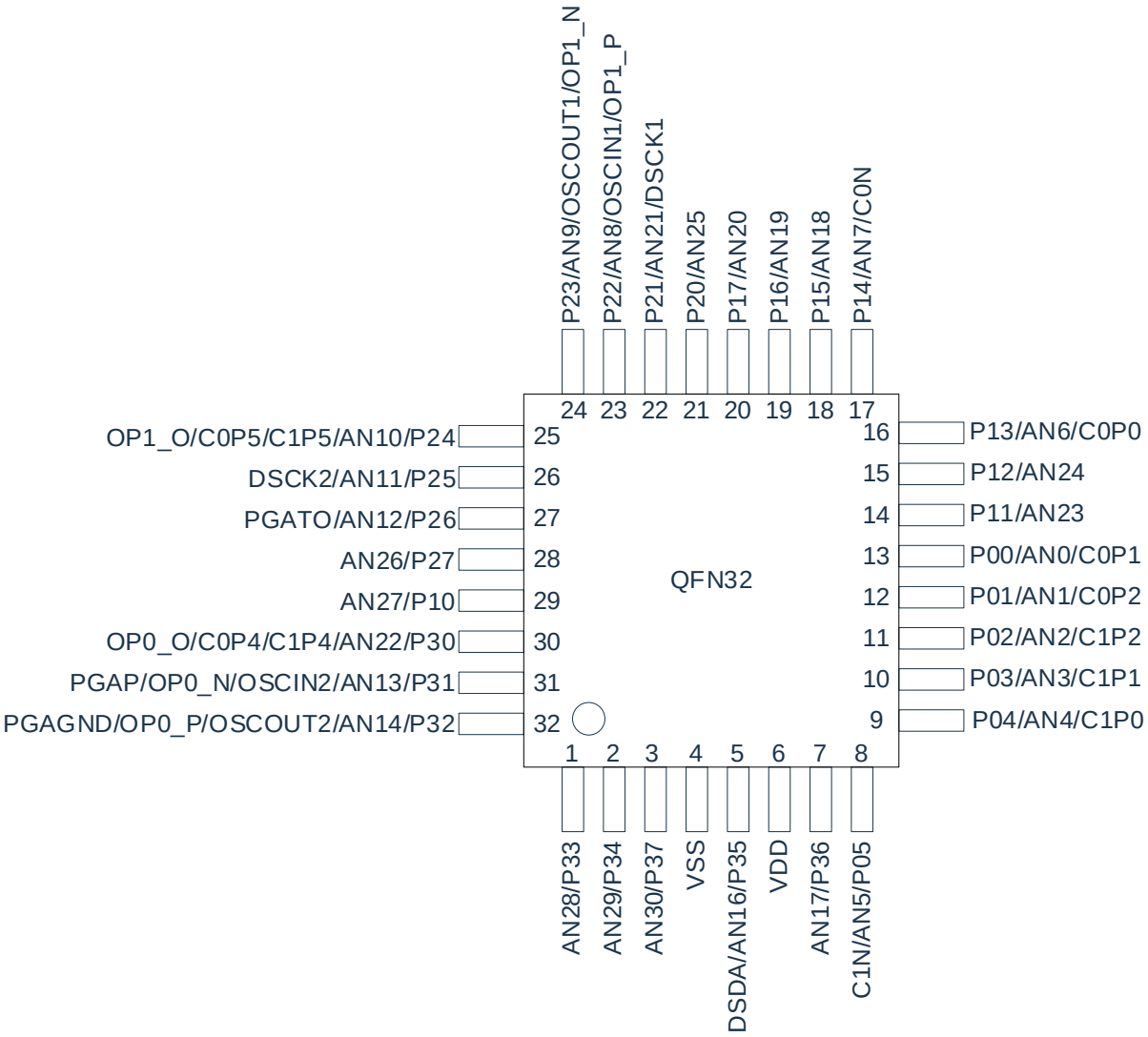
3.1.3 CMS8S006DC24NA



3.1.4 CMS8S006DC32FP



3.1.5 CMS8S006DC32NA



3.2 Pin function description

Pin number					Pin function	Pin type	Pin description
TSSOP 20	SSOP 24	QFN 24	LQFP 32	QFN 32			
-	16	16	13	13	P00	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN0	I	ADC channel 0 input
					C0P1	I	Comparator 0 positive terminal channel 1 input
-	15	15	12	12	P01	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN1	I	ADC channel 1 input
					C0P2	I	Comparator 0 positive channel 2 input
-	14	14	11	11	P02	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN2	I	ADC channel 2 input
					C1P2	I	Comparator 1 positive channel 2 input
-	13	13	10	10	P03	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN3	I	ADC channel 3 input
					C1P1	I	Comparator 1 positive channel 1 input
12	12	12	9	9	P04	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN4	I	ADC channel 4 input
					C1P0	I	Comparator 1 positive channel 0 input
11	11	11	8	8	P05	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN5	I	ADC channel 5 input
					C1N	I	Comparator 1 negative channel input
-	-	-	29	29	P10	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN27	I	ADC channel 27 input
-	-	-	14	14	P11	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN23	I	ADC channel 23 input
-	-	-	15	15	P12	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN24	I	ADC channel 24 input
13	17	17	16	16	P13	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN6	I	ADC channel 6 input
					C0P0	I	Comparator 0 positive channel 0 input
14	18	18	17	17	P14	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN7	I	ADC channel 7 input
					C0N	I	Comparator 0 negative channel input
15	19	19	18	18	P15	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN18	I	ADC channel 18 input
16	20	20	19	19	P16	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN19	I	ADC channel 19 input
17	21	21	20	20	P17	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN20	I	ADC channel 20 input
-	-	-	21	21	P20	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN25	I	ADC channel 25 input
18	22	22	22	22	P21	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN21	I	ADC channel 21 input
					DSCK1	I/O	Dual-line programming, debug clock input and output channel 1

Pin number					Pin function	Pin type	Pin description
TSSOP 20	SSOP 24	QFN 24	LQFP 32	QFN 32			
19	23	23	23	23	P22	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN8	I	ADC channel 8 input
					OSCIN1	I	External oscillator 1 input
					OP1_P	I	Op-amp 1 positive input
20	24	24	24	24	P23	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN9	I	ADC channel 9 input
					OSCOUT1	O	External oscillator 1 output
					OP1_N	I	Op-amp 1 negative input
1	1	1	25	25	P24	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN10	I	ADC channel 10 input
					C0P5	I	Comparator 0 positive channel 5 input
					C1P5	I	Comparator 1 positive channel 5 input
					OP1_O	O	Op-amp 1 output
2	2	2	26	26	P25	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN11	I	ADC channel 11 input
					DSCK2	I/O	Dual-line programming, debug clock input and output channel 2
3	3	3	27	27	P26	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN12	I	ADC channel 12 input
					PGATO	O	PGA test output
-	-	-	28	28	P27	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN26	I	ADC channel 26 input
4	4	4	30	30	P30	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN22	I	ADC channel 22 input
					C0P4	I	Comparator 0 positive channel 4 input
					C1P4	I	Comparator 1 positive channel 4 input
					OP0_O	O	Op-amp 0 output
5	5	5	31	31	P31	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN13	I	ADC channel 13 input
					OSCIN2	I	External oscillator 2 input
					OP0_N	I	Op-amp 0 negative input
					PGAP	I	PGA positive input
6	6	6	32	32	P32	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN14	I	ADC channel 14 input
					OSCOUT2	O	External oscillator 2 output
					OP0_P	I	Op-amp 0 positive input
					PGAGND	I	PGA feedback ground input
-	-	-	1	1	P33	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN28	I	ADC channel 28 input
-	-	-	2	2	P34	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN29	I	ADC channel 29 input
8	8	8	5	5	P35	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN16	I	ADC channel 16 input
					DSDA	I/O	Dual-line programming, debug data input and output
10	10	10	7	7	P36	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
					AN17	I	ADC channel 17 input
-	-	-	3	3	P37	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions

Pin number					Pin function	Pin type	Pin description
TSSOP 20	SSOP 24	QFN 24	LQFP 32	QFN 32			
					AN30	I	ADC channel 30 input
9	9	9	6	6	VDD	P	Power supply voltage input pin
7	7	7	4	4	VSS	P	Ground pin

3.3 GPIO features

The GPIO pins support multiple shared functions, with each I/O port configurable for any digital function or specified analog function. As general-purpose GPIO ports, they have the following features:

- Configurable for two output speed levels.
- Configurable for two drive current levels.
- Ability to read the status of data latches or pin states.
- Configurable for TTL level input or Schmitt trigger input.
- Configurable for interrupt triggering on rising edge, falling edge, or both edges.
- Configurable for interrupt wake-up on rising edge, falling edge, or both edges.
- Configurable as normal input, pull-up input, pull-down input, push-pull output, or open-drain output mode.

3.4 Pin function list

The CMS8S006 series chip allows arbitrary assignment of digital functions to its pins, meaning each I/O port can be assigned any digital function. The assignable digital functions are listed in the table below:

Digital function	Direction	Function description
GPIO	I/O	GPIO configured through registers for input, output, pull-up, and pull-down functions
CC0	O	Timer2 compare output channel 0
CC1	O	Timer2 compare output channel 1
CC2	O	Timer2 compare output channel 2
CC3	O	Timer2 compare output channel 3
TXD0	O	UART0 data output
RXD0	I/O	UART0 data input/synchronous mode data output
TXD1	O	UART1 data output
RXD1	I/O	UART1 data input/synchronous mode data output
SCL	I/O	I^2C clock input/output
SDA	I/O	I^2C data input/output
NSS	I/O	SPI slave mode chip select signal (input/output)
SCLK	I/O	SPI clock input/output
MOSI	I/O	SPI master transmit/slave receive
MISO	I/O	SPI master receive/slave transmit
PG0	O	PWM channel 0 output
PG1	O	PWM channel 1output
PG2	O	PWM channel 2 output
PG3	O	PWM channel 3 output
PG4	O	PWM channel 4 output
PG5	O	PWM channel 5 output
BEEP	O	Buzzer drive output
C0_O	O	Comparator 0 output
C1_O	O	Comparator 1 output
INT0	I	External interrupt 0 input
INT1	I	External interrupt 1 input
T0	I	Timer0 external clock input
T0G	I	Timer0 gate input
T1	I	Timer1 external clock input
T1G	I	Timer1 gate input
T2	I	Timer2 external event or gate input
T2EX	I	Timer2 falling edge auto reload input
CAP0	I	Timer2 input capture channel 0
CAP1	I	Timer2 input capture channel 1
CAP2	I	Timer2 input capture channel 2
CAP3	I	Timer2 input capture channel 3

Digital function	Direction	Function description
ADET	I	ADC external trigger input
FB	I	PWM external brake signal input

The allocation of analog functions for the pins is fixed, with each pin assigned a different analog function. The actual pin assignments are based on the specific product. The allocation of analog functions is shown in the table below:

PIN	CONFIG	1(ANALOG)				Other digital function priority
P00	-	AN0	C0P1	-	-	Highest
P01	-	AN1	C0P2	-	-	
P02	-	AN2	C1P2	-	-	
P03	-	AN3	C1P1	-	-	
P04	-	AN4	C1P0	-	-	
P05	-	AN5	C1N	-	-	
P10		AN27	-	-	-	
P11		AN23	-	-	-	
P12		AN24	-	-	-	
P13	-	AN6	C0P0	-	-	
P14	-	AN7	C0N	-	-	
P15	-	AN18	-	-	-	
P16	-	AN19	-	-	-	
P17	-	AN20	-	-	-	
P20		AN25	-	-	-	
P21	DSCK1	AN21	-	-	-	
P22	OSCIN1	AN8	-	OP1_P	-	
P23	OSCOUT1	AN9	-	OP1_N	-	
P24	-	AN10	C0P5/C1P5	OP1_O	-	
P25	DSCK2	AN11	-	-	-	
P26	-	AN12	-	-	PGATO	
P27		AN26	-	-	-	
P30	-	AN22	C0P4/C1P4	OP0_O	-	
P31	OSCIN2	AN13	-	OP0_N	PGAP	
P32	OSCOUT2	AN14	-	OP0_P	PGAGND	
P33		AN28	-	-	-	
P34		AN29	-	-	-	
P35	DSDA	AN16	-	-	-	
P36	-	AN17	-	-	-	
P37		AN30	-	-	-	Lowest

4. Function Summary

4.1 System clock

The system clock is controlled through the settings of the system configuration register and the oscillator control register, allowing for clock source and clock division selection. The chip clock source can be selected from the following four types:

- Internal high-speed oscillator (HSI) (48 MHz).
- External high-speed oscillator (HSE) (8 MHz/16 MHz).
- External low-speed oscillator (LSE) (32.768 kHz).
- Internal low-speed oscillator (LSI) (125 kHz).

4.2 Reset

Reset operations are used to initialize the internal circuits of the chip, allowing the system to start from a defined state. The chip has the following types of reset:

- Power-on reset.
- External reset.
- Low voltage reset.
- Watchdog overflow reset.
- Windowed watchdog reset.
- Software reset.
- CONFIG state protection reset.
- Power-on configuration monitoring reset.

Any of the above reset situations require a certain response time, and the system provides a comprehensive reset process to ensure the smooth execution of the reset actions.

4.3 Power management

4.3.1 Operating mode

The chip has four different operating modes to accommodate various power consumption needs for different applications:

- Normal mode

  The MCU operates in normal mode, with peripherals functioning as expected.

- Idle mode 1 (IDLE1)

  In this mode, the MCU is in Idle Mode 1 (IDLE1), where the CPU stops working, but both digital and analog peripherals continue to operate. This mode can be awakened by any interrupt.

- Idle mode 2 (IDLE2)

  In Idle Mode 2 (IDLE2), the MCU's CPU is stopped, while digital peripherals continue to function. The enable bits for analog peripherals (ADC/OPA/ACMP/PGA) are forcibly disabled. This mode can be awakened by any interrupt except for ADC and ACMP interrupts.

- Sleep mode (STOP)

  In sleep mode (STOP), the MCU halts all operations, with both digital and analog peripherals turned off. This mode can be awakened by INT0/1 interrupts, external interrupts, WUT timer wake-up, LSE timer wake-up, or WWDT timer wake-up.

4.3.2 Low voltage reset (LVR)

When the power supply voltage falls below the set detection voltage, the system will reset.

There are four options for the low voltage reset: 1.8V, 2.0V, and 2.5V.

4.3.3 Low voltage detection (LVD)

This series of products contains a low-voltage detection circuit that can compare the power supply voltage with the set detection voltage. If the power supply voltage is lower than the set detection voltage, an interrupt request signal is generated.

There are 8 options for detection voltage: 2.0V/2.2V/2.4V/2.7V/3.0V/3.7V/4.0V/4.3V.

4.4 Interrupt control

The chip features multiple interrupt sources and interrupt vectors. User-configurable interrupts include INT0/1, Timer0/1, Timer2, Timer3/4, WDT, LSE_Timer, PWM, I2C, SPI, UART0/1, P0/P1/P2/P3, ADC, and WWDT. The actual number of interrupt sources may vary by product.

The chip supports two interrupt priority levels, allowing for two-level interrupt nesting. If an interrupt is currently being serviced and a higher-priority interrupt request occurs, the latter can interrupt the former, enabling nested interrupts.

4.5 Timers

4.5.1 WDT

The Watchdog Timer (WDT) is an on-chip timer that uses the system clock as its time source. A WDT overflow will trigger a reset. The watchdog reset serves as a protective mechanism for the system, allowing it to reset in case it enters an unknown state, thus preventing it from getting stuck in an infinite loop. The WDT timer has the following features:

- Eight selectable WDT overflow timing levels.
- Configurable watchdog overflow interrupt.
- Configurable watchdog overflow reset.

4.5.2 WWDT

The Windowed Watchdog Timer (WWDT) is a 5-bit down-counting timer that uses a clock source provided by LSI and offers selectable prescaler options. By clearing the timer within a designated window period, it prevents the system from entering an indefinite loop due to erroneous states. This timer can generate interrupts, wake the system from sleep mode, and reset the chip. The WWDT timer has the following features:

- Five selectable windowed comparison times.
- Configurable windowed watchdog overflow interrupt.
- Configurable windowed watchdog overflow reset.

4.5.3 Timer 0/1

Timer 0 and Timer 1 share similar types and structures, both functioning as 16-bit up-counting timers. Timer 0 offers four operational modes, while Timer 1 provides three, enabling basic timing and event counting operations.

In timer mode, the timer register increments every 12 or 4 system cycles when the timer clock is enabled. In counter mode, the timer register increments upon detecting a falling edge on the corresponding input pins (T0, T1, PWM0). Timer 0/1 has the following features:

- Can be used as a normal timer.
- Supports gated timing functionality.
- Supports external counting functionality.
- Supports gated counting functionality.
- Generates counter overflow interrupts.

4.5.4 Timer 2

Timer 2 is a 16-bit timer designed for generating various digital signals and event capturing, such as pulse generation, pulse width modulation, and pulse width measurement. Timer 2 has the following features:

- Can be used as a normal timer.
- Supports gated timing functionality.
- Supports external counting functionality.
- Includes reload-disable, automatic overflow reload, and automatic reload on external pin falling edge.
- Can trigger capture on rising edge, falling edge, both edges, or writing to the low byte of the capture register.
- Features a comparison function that can generate periodic signals with controllable duty cycle PWM waveforms.
- Supports interrupts for timing, external triggers, capture, and comparison operations.
- Supports continuous capture mode.

4.5.5 Timer 3/4

Timer 3 and Timer 4 are similar to Timer 0 and Timer 1, functioning as two 16-bit timers. Timer 3 has four operating modes, while Timer 4 has three operating modes. Unlike Timer 0 and Timer 1, Timer 3 and Timer 4 only provide timer operations.

When the timers are started, the values in the registers (counters) increment once every 12 or 4 system cycles.

4.5.6 LSE timer

The LSE timer is a 16-bit up-counting timer with a clock source derived from an external low-speed clock (LSE). The LSE timer has the following features:

- Timing functionality.
- Supports setting a 16-bit timing value.
- Can operate normally in sleep mode.
- Generates an interrupt when the count value equals the timing value.
- Timing interrupts can wake the device from idle mode 1/2 (IDLE1/2) sleep modes.

4.5.7 WUT

The WUT (Wake-Up Timer) is a 12-bit up-counting timer with a clock source derived from the internal low-speed clock (LSI), designed for waking the system from sleep mode. After the system enters sleep mode, the CPU and all peripheral circuits stop working, while the internal low-speed clock LSI provides the clock for the WUT counter. The WUT has the following features:

- Can wake the system from sleep state.
- Count clock can be configured with division factors of 1, 8, 32, or 256.
- Supports setting a 12-bit timing value.

4.5.8 BRT

The BRT (Baud Rate Timer) is a 16-bit timer with a clock source derived from the system clock, primarily providing clock signals for the UART module. The BRT has the following features:

- Independent control switch.
- Count clock with 8 selectable division factors.
- 16-bit incremental counting.

4.6 Enhanced digital peripherals

4.6.1 Buzzer

The buzzer driver consists of an 8-bit counter, a clock driver, and a control register, generating a square wave with a 50% duty cycle and a broad frequency range. The BUZZER has the following features:

- Independent enable control switch.
- Selectable system clock division ratios of 8, 16, 32, and 64.
- Output frequency controlled by an 8-bit value, adjustable from (1 to 255) x 2 division output.

4.6.2 Multiplication and division unit (MDU)

The MDU module has the following features:

- Supports 32bit/16bit division.
- Supports 16bit/16bit division.
- Supports 16bit×16bit multiplication.
- Supports 32bit shift operations.
- Supports normalization operations.

4.6.3 Enhanced PWM module

The enhanced PWM module supports six PWM generators, with independent configuration for period and duty cycle. The PWM module features:

- Supports two waveform output modes: one-shot and continuous.
- Supports four control modes: independent, complementary, synchronous, and group control.
- Selectable counting clock division factors of 1, 2, 4, 8, and 16.
- Supports two counting modes: edge-aligned and center-aligned, with symmetric and asymmetric counting in center-aligned mode.
- Supports mask output.
- Supports dead time programming.
- Configurable output polarity.
- Supports period, up-count comparison, down-count comparison, and zero-point interrupts.
- Supports software brake, external port trigger brake, ADC comparison result trigger brake, and ACMP output trigger brake.
- Supports four fault recovery modes.

4.7 Communication module

4.7.1 SPI module

The SPI (Serial Peripheral Interface) is a fully configurable master/slave device that allows users to configure the polarity and phase of the serial clock signal. SPI enables communication between the MCU and serial peripheral devices, and it can also facilitate inter-processor communication in multi-master systems. The SPI features include:

- Full-duplex synchronous serial data transmission.
- Supports master/slave modes.
- Supports multi-master systems.
- System error detection.
- Supports speeds up to 1/4 of the system clock (F_{SYS} ≤ 24MHz).
- Bit rates generated at 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, and 1/512 of the system clock.
- Supports four transmission formats.
- Interrupt generation upon completion of transmit/receive operations.

4.7.2 I²C module

The I²C module is a two-wire bidirectional serial bus controller that provides a simple and efficient means for data exchange between microprocessors and I²C buses. The I²C module features include:

- Supports four operating modes: master transmit, master receive, slave transmit, and slave receive.
- Supports two transmission speed modes:
  Standard mode (up to 100 Kb/s)
  Fast mode (up to 400 Kb/s)
- Handles arbitration and clock synchronization.
- Supports multi-master systems.
- Master mode supports 7-bit and 10-bit addressing modes on the I²C bus (software supported).
- Slave mode supports 7-bit addressing on the I²C bus.
- Allows operation over a wide clock frequency range (with built-in 8-bit timer).
- Interrupt generation upon completion of receive/transmit operations.

4.7.3 UARTn module

The UARTn module includes UART0 and UART1. The UARTn features include:

- Full-duplex serial port.
- Supports synchronous mode.
- Supports variable baud rate in 8-bit asynchronous transmission mode.
- Supports variable baud rate in 9-bit asynchronous transmission mode.
- Baud rate can be generated by Timer1, Timer4, Timer2, or the BRT module.
- Interrupt generation upon completion of transmit/receive operations.

4.8 Analog module

4.8.1 Analog-to-digital converter (ADC)

The ADC module is a 12-bit successive approximation analog-to-digital converter. The port's analog input signals are connected to the ADC input through a multiplexer, and the ADC generates a 12-bit binary result based on the input analog signal, storing this result in the ADC result register. The ADC features include:

- All I/O ports can serve as external input channels for the ADC.
- 15 selectable clock frequencies for ADC conversion.
- ADC reference voltage options: 2.0V, 2.4V, 3.0V, or VDD.
- Selectable sample-and-hold time (4/8 TADCK).
- Supports averaging of conversion results over 1, 4, 8, or 16 conversions.
- Enhanced PWM triggering for ADC conversion via external port edges.
- Supports comparison output of ADC conversion results, which can control enhanced PWM braking functionality.
- Interrupt generation upon completion of ADC conversion.
- Supports accumulation of results from multiple conversions.

4.8.2 Analog comparators (ACMP0/1)

The comparators ACMP0 and ACMP1 feature the following characteristics:

- Positive input supports multiple selectable input ports.
- Negative input can be selected from port input or internal reference voltage.
- Internal reference voltage divider has 16 selectable levels.
- Supports output filtering with 11 selectable filter time options.
- Supports single-side and double-side hysteresis control.
- Hysteresis voltage options: 10mV, 20mV, or 60mV.
- Output can serve as a braking trigger signal for enhanced PWM.
- Supports interrupt generation upon output change.
- Supports output latching functionality.

4.8.3 Operational amplifiers (OP0/1)

The operational amplifiers feature the following characteristics:

- Positive input supports internal 1.2V voltage.
- Supports both comparator and operational amplifier modes.
- Output can be connected to the internal ACMP input for shaping.
- Output can also be connected to ADC channel 31 for measurement.

4.8.4 Programmable gain amplifier (PGA)

The programmable gain amplifier (PGA) features the following characteristics:

- Multiple selectable gains (1, 2, 4, 8, 16, 32, 64, 128).
- Supports single-ended and pseudo-differential inputs.
- Supports PGA output testing.
- PGA output can be connected to the internal analog comparator input for shaping.

4.9 FLASH memory

The FLASH memory includes program memory (APROM) and non-volatile data memory (Data FLASH). Access operations can be performed through related Special Function Registers (SFR) to enable In-Application Programming (IAP) functionality. FLASH memory supports the following operations:

- Byte read operations.
- Byte write and continuous byte write operations.
- Page erase operations.

4.10 Unique ID (UID)

Each chip has a 96-bit unique identification number, known as the Unique ID (UID). The UID is set at the factory and cannot be modified by the user.

5. User Configuration

The System Configuration Register (CONFIG) contains the FLASH options for the MCU's initial conditions and cannot be accessed or modified by the program. The following settings can be configured through the System Configuration Register:

- Watchdog operating mode.
- FLASH program area partition protection, code encryption, FLASH data area partition protection, encryption status.
- Low voltage reset threshold.
- Debug mode enable or disable.
- Oscillation mode and prescaler selection.
- Internal high-speed oscillator divider selection.
- External reset configuration and port selection.
- Sleep wake-up wait time.

6. Electrical Characteristics

6.1 Absolute maximum ratings

Unless otherwise specified, the temperature condition for the following parameters is T_A =25℃.

Symbol	Parameter	Min.	Max.	Unit
T_{ST}	Storage temperature	-55	150	℃
T_A	Operating temperature	-40	85	℃
VDD-VSS	Power supply voltage	-0.3	5.8	V
V_{IN}	Input voltage	VSS-0.3	VDD+0.3	V
I_{DD}	V_{DD} maximum input current	-	120	mA
I_{SS}	V_{SS} maximum output current	-	120	mA
I_{IO}	Maximum sink current of a single I/O	-	50	mA
	Maximum source current of a single I/O	-	40	mA
	Maximum sink current of all I/Os	-	120	mA
	Maximum source current of all I/Os	-	120	mA

Caution: Operating the device beyond the "**Absolute Maximum Ratings**" range will cause permanent damage. Functionality is guaranteed only when the device operates within the specified range in the manual. Operating the chip under absolute maximum ratings conditions may affect the device's reliability.

6.2 DC electrical parameters

VDD-VSS=2.1~5.5V, T_A=25℃

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VDD	Operating voltage	F_{SYS}=48MHz, machine cycle=3T F_{SYS}=24MHz, machine cycle=2T F_{SYS}=8MHz~16MHz, machine cycle=1T	2.1	-	5.5	V
I_{DD}	Normal mode	VDD=5V, F_{SYS}=48MHz, all peripherals off machine cycle=3T	-	6	-	mA
		VDD=3V, F_{SYS}=48MHz, all peripherals off machine cycle=3T	-	6	-	mA
		VDD=5V, F_{SYS}=24MHz, all peripherals off machine cycle=2T	-	4	-	mA
		VDD=3V, F_{SYS}=24MHz, all peripherals off machine cycle=2T	-	4	-	mA
		VDD=5V, F_{SYS}=16MHz, all peripherals off machine cycle=1T	-	3.5	-	mA
		VDD=3V, F_{SYS}=16MHz, all peripherals off machine cycle=1T	-	3.5	-	mA
		VDD=5V, F_{SYS}=8MHz, all peripherals off machine cycle=1T	-	2.5	-	mA
		VDD=3V, F_{SYS}=8MHz, all peripherals off machine cycle=1T	-	2.5	-	mA
	IDLE1	VDD=5V, F_{SYS}=48MHz, all peripherals off	-	4.5	-	mA
		VDD=3V, F_{SYS}=48MHz, all peripherals off	-	4.5	-	mA
		VDD=5V, F_{SYS}=24MHz, all peripherals off	-	3	-	mA
		VDD=3V, F_{SYS}=24MHz, all peripherals off	-	3	-	mA
		VDD=5V, F_{SYS}=16MHz, all peripherals off	-	2.5	-	mA
		VDD=3V, F_{SYS}=16MHz, all peripherals off	-	2.5	-	mA
		VDD=5V, F_{SYS}=8MHz, all peripherals off	-	2	-	mA
		VDD=3V, F_{SYS}=8MHz, all peripherals off	-	2	-	mA
	IDLE2	VDD=5V, F_{SYS}=125KHz, all peripherals off		15		uA
		VDD=3V, F_{SYS}=125KHz, all peripherals off		15		uA
		VDD=5V, F_{SYS}=32.768KHz, all peripherals off		20		uA
		VDD=3V, F_{SYS}=32.768KHz, all peripherals off		20		uA
I_{SLEEP1}	Sleep current	All peripherals off, LSE, LSE timer enabled	-	20	-	uA
I_{SLEEP2}	Sleep current	All peripherals off, LSI, WUT timer enabled	-	7	-	uA
I_{SLEEP3}	Sleep current	All peripherals off	-	6	-	uA
I_{LI}	Input leakage current	-	-	-	0.1	uA
V_{IL}	Input level, low	-	VSS	-	0.3VDD	V
V_{IH}	Input level, high	-	0.7VDD	-	VDD	V
V_{OL}	Output voltage, low	VDD=5V, I_{OL1}=12mA	-	-	0.4	V
		VDD=5V, I_{OL2}=7mA	-	-	0.4	V
		VDD=3V, I_{OL1}=9mA	-	-	0.4	V
		VDD=3V, I_{OL2}=5mA	-	-	0.4	V
V_{OH}	Output voltage, high	VDD=5V, I_{OH1}=40mA	3.5	-	-	V
		VDD=5V, I_{OH2}=20mA	3.5	-	-	V
		VDD=3V, I_{OH1}=15mA	2.1	-	-	V
		VDD=3V, I_{OH2}=8mA	2.1	-	-	V
R_{PH}	Pull-up	-	-	32	-	KΩ

	resistance					
R_{PL}	Pull-down resistance	-	-	32	-	KΩ

6.3 AC electrical parameters

6.3.1 Power-on reset time

T_A=25℃, excluding the reset time of the 32.768K crystal oscillator.

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{RESET}	Reset time	VDD=5V	-	18	-	ms
TVDDR	VDD rise rate	VDD=5V	20	-	-	us/V
TVDDF	VDD fall rate	VDD=5V	20	-	-	us/V

6.3.2 External oscillator

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{HSE}	Operating voltage	F=8/16MHz, C_{XT}=0-47pF	2.1	-	5.5	V
V_{LSE}	Operating voltage	F=32.768KHz, C_{XT}=10-22pF	2.1	-	5.5	V

6.3.3 Internal oscillator

VDD=2.1V-5.5V

Symbol	Parameter	Test condition	Frequency error	Min.	Typ.	Max.	Unit
F_{HSI}	Internal high-speed 48MHz	T_A=25℃	±1%	-	48	-	MHz
		T_A=-40℃ to 85℃	±3.5%	-	48	-	MHz
F_{LSI}	Internal low-speed 125KHz	T_A=25℃	±10%	-	125	-	KHz
		T_A=-40℃ to 85℃	±15%	-	125	-	KHz

6.3.4 Low-voltage reset electrical parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{LVR1}	Low voltage detection threshold value: 1.8V	1.65	1.8	2.0	V
V_{LVR2}	Low voltage detection threshold value: 2.0V	1.85	2.0	2.2	V
V_{LVR3}	Low voltage detection threshold value: 2.5V	2.35	2.5	2.8	V

6.3.5 LVD electrical parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{LVD1}	Low voltage detection threshold value: 2.0V	1.85	2.0	2.15	V
V_{LVD2}	Low voltage detection threshold value: 2.2V	2.05	2.2	2.35	V
V_{LVD3}	Low voltage detection threshold value: 2.4V	2.25	2.4	2.55	V
V_{LVD4}	Low voltage detection threshold value: 2.7V	2.55	2.7	2.85	V
V_{LVD5}	Low voltage detection threshold value: 3.0V	2.85	3.0	3.15	V
V_{LVD6}	Low voltage detection threshold value: 3.7V	3.55	3.7	3.85	V
V_{LVD7}	Low voltage detection threshold value: 4.0V	3.85	4.0	4.15	V
V_{LVD8}	Low voltage detection threshold value: 4.3V	4.15	4.3	4.45	V

6.4 FLASH electrical parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_F	FLASH operating voltage	-	2.1	-	5.5	V
T_F	FLASH operating temperature	-	-40	25	85	℃
$N_{ENDURANCE}$	Erase count	Program FLASH	20,000	-	-	Cycle
		Data FLASH	100,000	-	-	Cycle
T_{RET}	Data retention time	25℃	100	-	-	year
T_{ERASE}	Sector erasing time	-	-	2.5	-	ms
T_{WRITE}	Writing time	-	-	140	-	us
T_{READ}	Reading time	-	-	3*Tsys	-	-
I_{DD1}	Reading current	-	-	-	2.5	mA
I_{DD2}	Programming current	-	-	-	3.6	mA
I_{DD3}	Erasing current	-	-	-	2	mA

6.5 Analog circuit characteristics

6.5.1 BANDGAP electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{BG}	Internal reference 1.2V	V_{DD}=2.1~5.5V, T_A=25℃	1.188	1.2	1.212	V
		V_{DD}=2.1~5.5V, T_A=-20℃ to 85℃	1.182	1.2	1.218	V
		V_{DD}=2.1~5.5V, T_A=-40℃ to 85℃	1.176	1.2	1.224	V

6.5.2 ADC electrical characteristics

T_A=25℃

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{AVDD}	ADC operating voltage		2.5	-	5.5	V
V_{REF1}	Reference voltage 1		-	V_{AVDD}	-	V
V_{REF2}	Reference voltage 2		1.985	2.0	2.015	V
V_{REF3}	Reference voltage 3		2.385	2.4	2.415	V
V_{REF4}	Reference voltage 4		2.985	3.0	3.015	V
V_{ADI}	Input voltage		0	-	V_{REF}	V
N_R	Resolution		12			Bit
DNL	Differential nonlinearity error (V_{REF}=V_{AVDD}=5V, T_{ADCK}=0.5us)		±2			LSB
INL	Integral nonlinearity error (V_{REF}=V_{AVDD}=5V, T_{ADCK}=0.5us)		±4			LSB
T_{ADCK}	ADC clock period	V_{REF}=VDD=5V	0.125	-	-	us
		V_{REF} =V_{REF2}/ V_{REF3}/V_{REF4}	2	-	-	us
T_{ADC}	ADC conversion time (sample and hold time: 4*T_{ADCK})		-	25	-	T_{ADCK}
F_S	Sampling rate (V_{REF}=V_{AVDD}=5V)		320			Ksps

6.5.3 ACMP electrical characteristics

T_A=25℃, V_{SENSE}=V_{IN+}-V_{IN-}, VDD=5V, V_{IN+}=1V, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Power supply voltage	-	2.1	-	5.5	V
I_Q	Quiescent current	V_{SENSE}=0.1V	-	0.2	0.3	mA
I_{SD}	Shutdown current	V_{SENSE}=0.1V	-	10	-	nA
T_A	Operating temperature	-	-40	25	85	℃
Input characteristics						
V_{OS}	Input offset voltage	-	-	±10	-	mV
V_{CM}	Common mode input voltage range	-40℃~85℃	-0.1	-	VDD-1.3	V
I_B	Input bias current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset current	V_{SENSE}=0mV	-	10	-	pA
V_{HYS}	Input hysteresis voltage	VDD=2.1~5.5V, V_{IN+}=0.5V	-	0 ±10 ±20 ±60	-	mV
Output characteristics						
V_{OH}	Maximum output voltage	-40℃~85℃	-	-	VDD	V
V_{OL}	Minimum output voltage	-40℃~85℃	0	-	-	V
Frequency characteristics						
A_{OL}	Open loop gain	-	-	85	-	dB
BW	Bandwidth	-	-	150	-	MHz
PSRR	Power supply rejection ratio	VDD=2.1~5.5V, V_{IN+}=1V, V_{SENSE}=0mV	-	80	-	dB
CMRR	Common mode rejection ratio	VDD=2.1~5.5V -40℃~85℃	-	90	-	dB
Transient characteristics						
T_{STB}	Stable time	-	-	-	5	μs
T_{PGD}	Response delay	V_{COM}=1V, V_{IN+}= V_{IN-} ±0.1V	-	50	100	ns

Note: This specification is guaranteed by the design.

6.5.4 OP electrical characteristics

T_A=25℃, V_{SENSE}=V_{IN+}-V_{IN-}, VDD=5V, VIN+=1V, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Power supply voltage	-	2.5	-	5.5	V
I_Q	Quiescent current	V_{SENSE}=0mV	-	0.75	1.2	mA
I_{SD}	Shutdown current	-	-	5	-	nA
T_A	Operating temperature	-	-40	25	85	℃
Input characteristics						
V_{OS}	Input offset voltage	-	-	±10	±1.0	mV
V_{CM}	Common mode input voltage range	-40℃~85℃	0	-	VDD-1.3	V
I_B	Input bias current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset current	V_{SENSE}=0mV	-	10	-	pA
Output characteristics						
C_{LOAD}	Capacitive load	-	-	30	-	pF
V_{OH}	Maximum output voltage	-40℃~85℃	-	-	VDD-0.3	V
V_{OL}	Minimum output voltage	-40℃~85℃	0.3	-	-	V
Frequency characteristics						
A_{OL}	Open loop gain	-	-	80	-	dB
BW	Bandwidth	R_{LOAD}=2K, C_{LOAD}=100pF	-	5	-	MHz
PSRR	Power supply rejection ratio	VDD=2.5~5.5V, V_{IN+}=1V, V_{SENSE}=0mV	-	75	-	dB
CMRR	Common mode rejection ratio	V_{IN+}=0.3~ (VDD-1.5) -40℃~85℃	-	90	-	dB
Transient characteristics						
SR	Slew rate	R_{LOAD} =2K, C_{LOAD} =100pF	-	±7	-	V/μs
T_{STB}	Stable time	-	-	-	2	μs

Note: This specification is guaranteed by the design.

6.5.5 PGA electrical characteristics

T_A=25℃, VDD=5V, V_{IN+}=0.01V, unless otherwise specified (G is the gain factor).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Power supply voltage	-	2.5	-	5.5	V
I_Q	Quiescent current	V_{OUT}=2V	-	0.5	0.7	mA
I_{SD}	Shutdown current	-	-	10	-	nA
T_A	Operating temperature	-	-40	25	85	℃
Input characteristics						
V_{OS}	Input offset voltage	-	-	±2.5	-	mV
V_{CM}	Common mode input voltage range	G=1	0.032	-	(VDD-1)/ G	V
		G=2	0.016			
		G=4	0.008			
		G=8	0.004			
		G=16	0.002			
		G=32, 64,128	0.001			
I_B	Input bias current	-	-	10	-	pA
I_{OS}	Input offset current	-	-	10	-	pA
Output characteristics						
EG	Gain error	G=1, 2, 4, 8, 16	-1	-	1	%
		G=32	-2	-	2	
		G=64,128	-4	-	4	
C_{LOAD}	Capacitive load	-	-	10	-	pF
V_{OH}	Maximum output voltage	-40℃~85℃	-	-	VDD-1	V
V_{OL}	Minimum output voltage	-40℃~85℃	0.032	-	-	V
Frequency characteristics						
BW	Bandwidth	C_{LOAD}=10pF, G=1	-	1.5	-	MHz
PSRR	Power supply rejection ratio	VDD=2.5~5.5V, G=16	-	80	-	dB
CMRR	Common mode rejection ratio	-40℃~85℃	-	80	-	dB
Transient characteristics						
SR	Slew rate	C_{LOAD}=10pF, G=32	-	10	-	V/μs
T_{STB}	Stable time	-	-	-	2	μs

Note: This specification is guaranteed by the design.

6.6 EMC characteristics

6.6.1 EFT electrical characteristics

Symbol	Parameter	Test condition	Grade
V_{EFTB}	Fast transient voltage burst limits to be applied through 0.1uF(capacitance) on V_{DD} and V_{SS} pins to induce a functional disturbance	T_A = + 25℃, F_{SYS}=48MHz, conforms to IEC 61000-4-4	4B

Note: The immunity performance against Electrical Fast Transient (EFT) pulses is closely related to system design aspects, including power supply structure, circuit design, layout and wiring, chip configuration, program structure, and more. The EFT parameters listed in the table are results obtained from testing on CMS internal testing platforms and may not apply universally to all application environments. These test data serve as reference only. Various aspects of system design can influence EFT performance. In applications where high EFT immunity is required, it is advisable to design while minimizing the impact of interference sources on system operation. It is recommended to analyze interference paths and optimize designs to achieve the best immunity performance against EFT disturbances.

6.6.2 ESD electrical characteristics

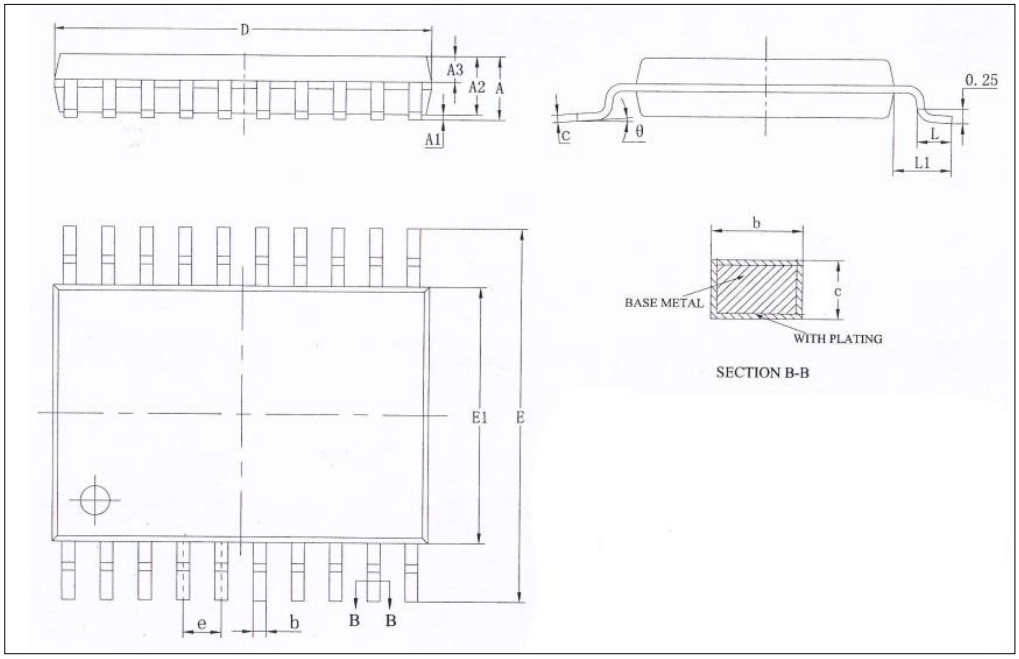
Symbol	Parameter	Test condition	Grade
V_{ESD}	Electrostatic discharge (Human-Body Model: HBM)	T_A = + 25℃, JEDEC EIA/JESD22- A114	3B
	Electrostatic discharge (Machine Model: MM)	T_A = + 25℃, JEDEC EIA/JESD22- A115	C

6.6.3 Latch-Up electrical characteristics

Symbol	Parameter	Test condition	Classification
LU	Static latch-up class	JEDEC STANDARD NO.78D NOVEMBER 2011	Class I (T_A = +25℃)

7. Package Dimensions

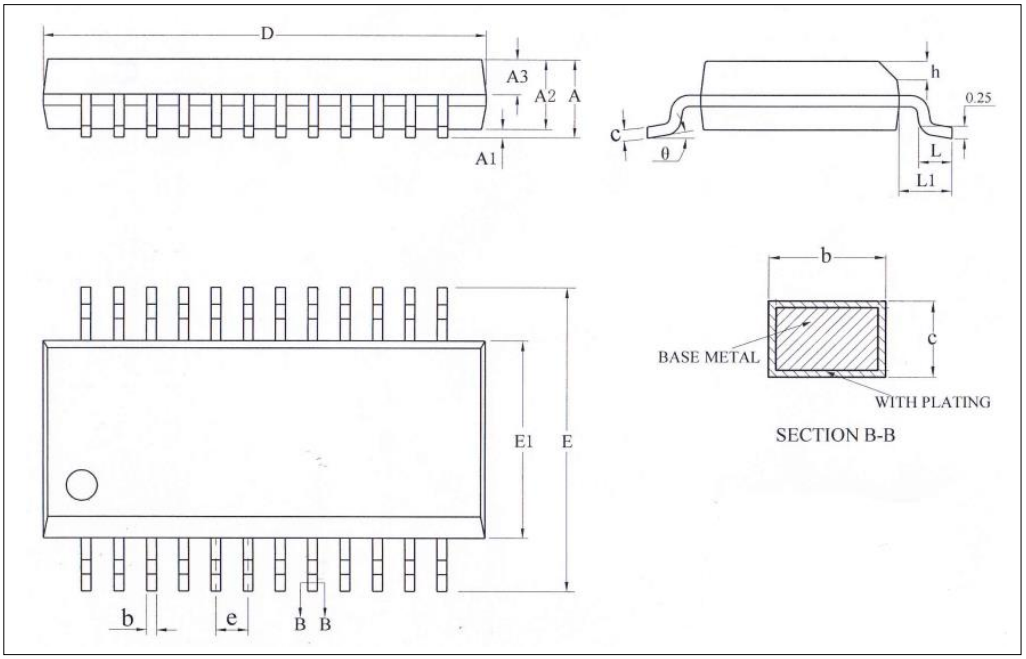
7.1 TSSOP20



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.25
A1	0.05	-	0.15
A2	0.80	1.00	1.10
A3	0.34	0.44	0.54
b	0.20	-	0.28
c	0.10	-	0.19
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	-	8°

Caution: Package dimensions do not include mold flash or gate burrs.

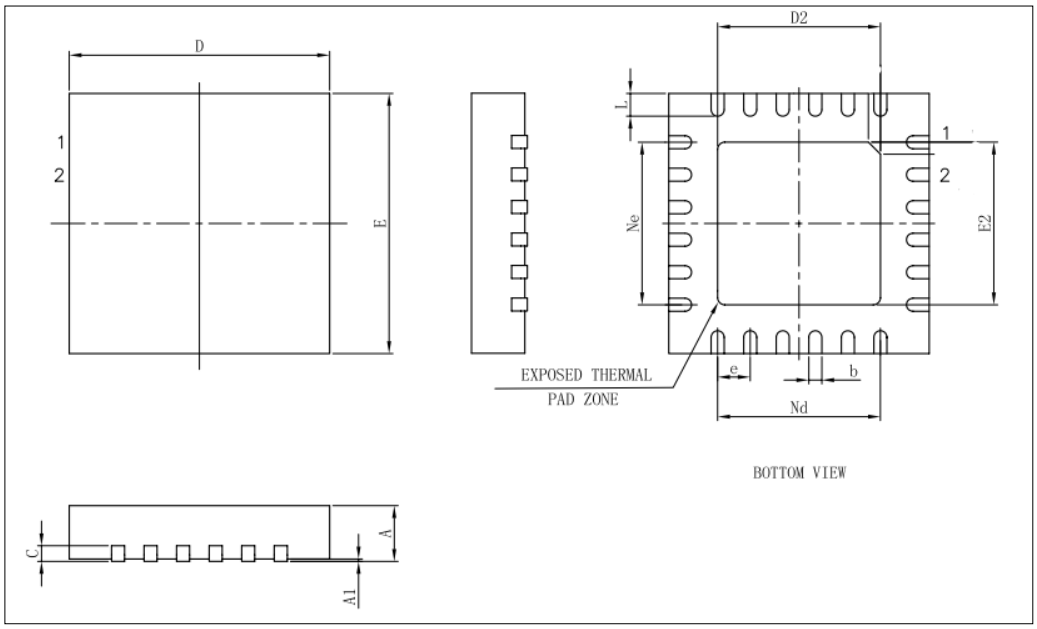
7.2 SSOP24



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.80
A1	0.10	0.15	0.25
A2	1.30	-	1.55
A3	0.60	0.65	0.70
b	0.20	-	0.31
c	0.20	-	0.24
D	8.53	-	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	-	0.50
L	0.406	-	0.889
L1	1.05REF		
θ	0	-	8°

Caution: Package dimensions do not include mold flash or gate burrs.

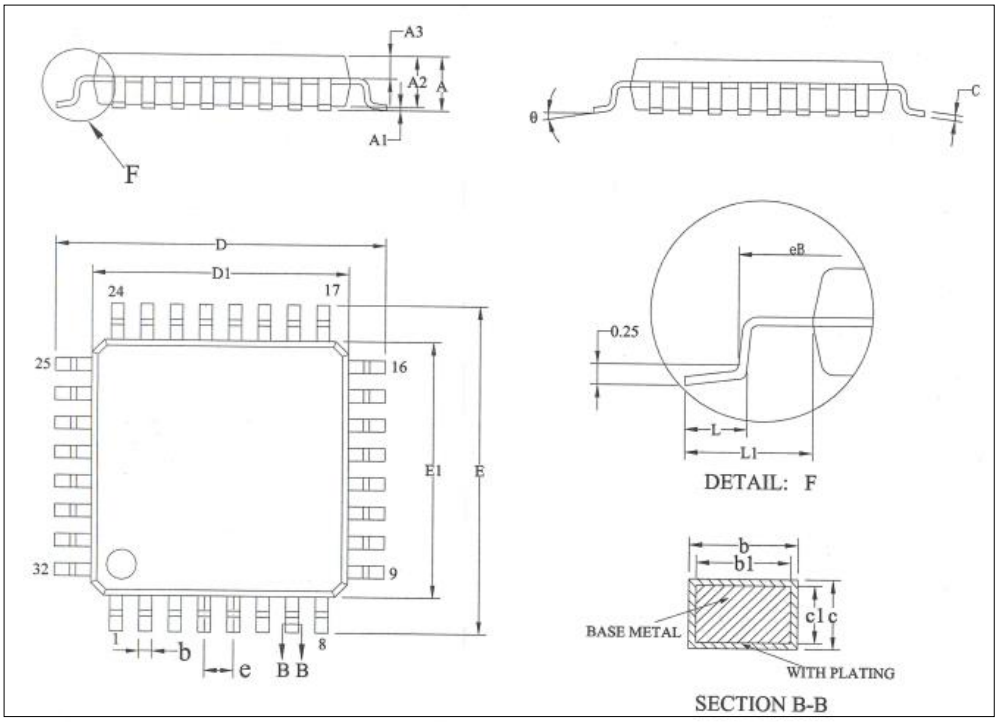
7.3 QFN24（4*4*0.75-0.50）



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.20	-	2.80
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.20	-	2.80
L	0.30	0.40	0.50
h	0.25	-	0.40

Caution: Package dimensions do not include mold flash or gate burrs.

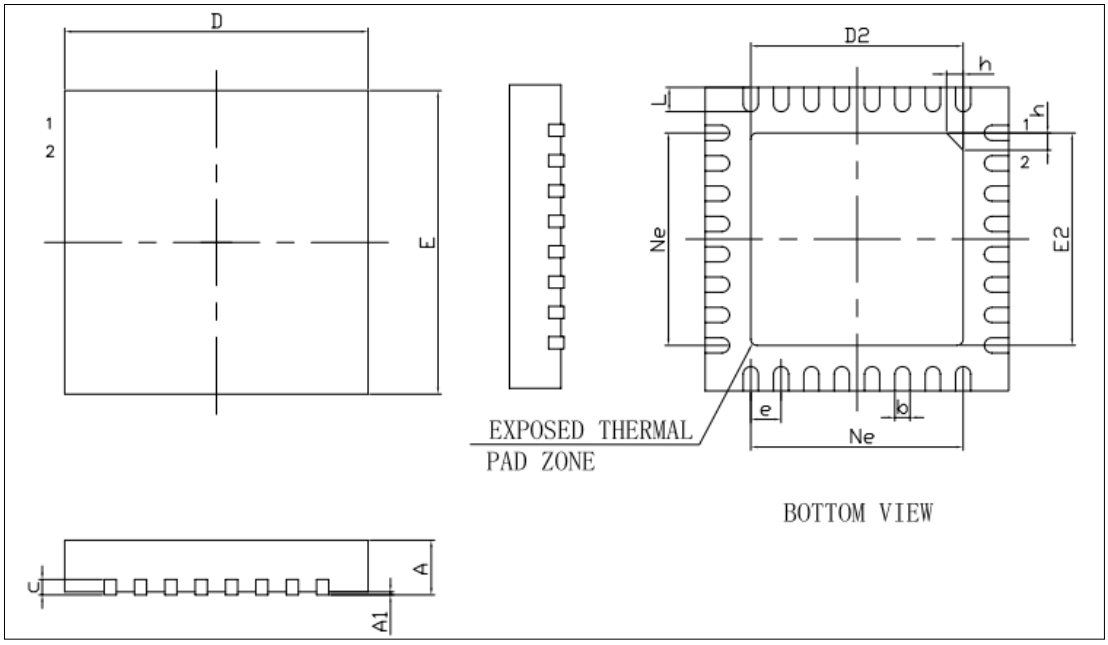
7.4 LQFP32（7*7）



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32	-	0.43
b1	0.31	-	0.39
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.80BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

Caution: Package dimensions do not include mold flash or gate burrs.

7.5 QFN32（5*5*0.75-0.50）



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	-	3.75
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	-	3.75
L	0.30	-	0.45
h	0.30	0.35	0.40

Caution: Package dimensions do not include mold flash or gate burrs.

8. Revision History

Version	Date	Description of changes
V0.1.0	Oct. 2023	Initial version
V0.1.1	Dec. 2023	Deleted model number CMS8S006DC20NB and related information
V0.1.2	Jan. 2024	1) Revised the low voltage reset value in sections 1.1/0/4.3.2 and 6.3.4 Low-voltage reset electrical parameters 2) Revised the internal high-speed oscillation frequency error in 6.3.3
V0.1.3	Feb. 2024	1) Modified input offset voltage parameters in 6.5.3/6.5.4/6.5.5 2) Revised the internal high-speed oscillation frequency error in 6.3.3 3) Deleted the description of “support for software trimming of the offset voltage” from the content.
V0.1.4	Oct. 2024	Modified TSSOP20/SSOP24/LQFP32/QFN32 package dimensions